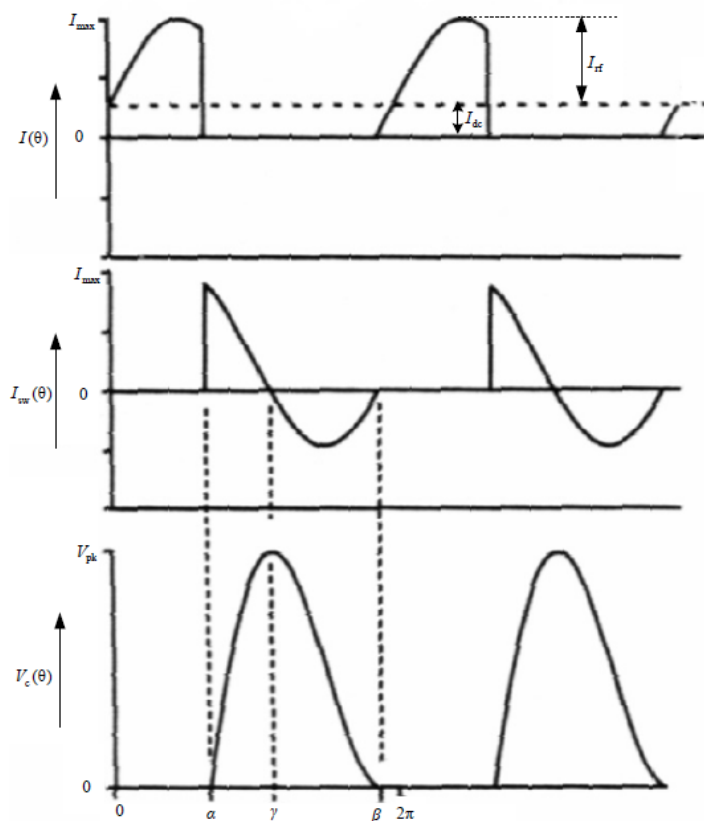


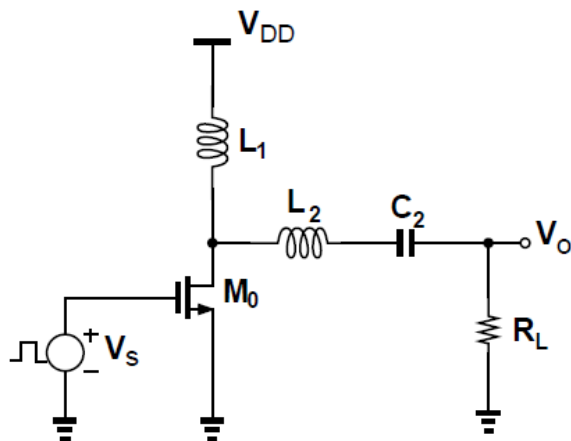
Class E Power Amplifier

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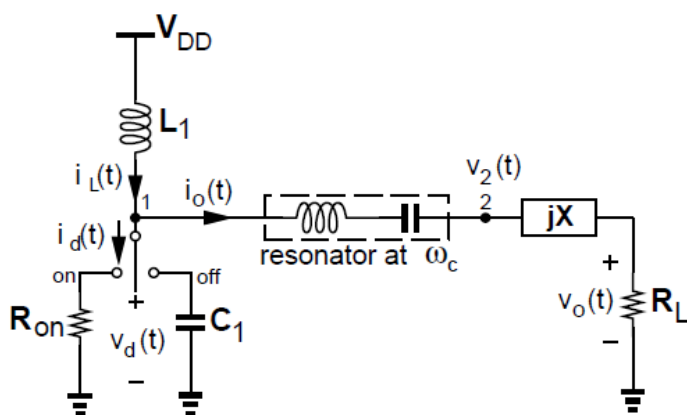
Class E 功率放大器是一种开关模式功率放大器，晶体管作为开关来使用。开关模式功率放大器（如 Class D、E、F 等）的基本思想是使器件输出端的电压、电流波形不重叠，从而器件上不耗散功率，使得功率放大器的效率很高。Class E 与 Class D 的不同之处在于，它通过对开关（器件）上的电压进行整形，使得在开关导通瞬间，开关上的电压和电压变化斜率都为 0（软开关），从而减小了开关在不完全导通过程中的损耗。但是，Class E 功率放大器没有对开关截止时开关上的电压波进行整形，因此，器件在不完全截止过程中的损耗仍然会降低放大器的效率。



下图所示为一个 CMOS Class E 功率放大器的电路原理图：



(a)



除了 NMOS 器件，电路还包括扼流电感 L_1 、匹配网络 L_2 及 C_2 、负载阻抗 R_L （一般为 50Ω ）。以下所有分析都基于三个假设：

- 当 NMOS 打开（on）时，NMOS 的导通电阻 R_{on} 恒定，并且是此时 NMOS 输出阻抗的主要组成部分，忽略其余参数影响；
- 当 NMOS 关闭（off）时，NMOS 的寄生电容 C_1 恒定，并且是此时 NMOS 输出阻抗的主要组成部分，忽略其余参数影响；
- 输出阻抗匹配网络的 Q 值 $Q = \frac{\omega_c L_2}{R_L}$ 很高，所以 Class E 输出为正弦波。
- 匹配网络 L_2 及 C_2 的理想谐振频率为 f_c ，其附加的超前相位由电抗

$$jX = j\omega_c L_2 + \frac{1}{j\omega_c C_2}$$

在大幅度方波信号的驱动下，输出信号为正弦周期信号，设信号频率为 $\omega_c = 2\pi/T$ ，输出电流为：

$$i_o(t) = I_o \sin(\omega_c t + \phi_0) \quad (1.1)$$

节点 2 的电压波形为正弦波型，但是附加一个由 jX 引入的附加超前相位：

$$v_2(t) = V \sin(\omega_c t + \phi_1) \quad (1.2)$$

其中， $V = I_o R_L \sqrt{1 + \frac{X^2}{R_L^2}}$ ， $\phi_1 = \phi_0 + \tan^{-1}(\frac{X}{R_L})$ 。

流过电感 L_1 的电流表示为：

$$i_L(t) = i_d(t) + I_o \sin(\omega_c t + \phi_0) \quad (1.3)$$

$$V_{DD} - v_d(t) = L_1 \frac{di_L(t)}{dt} \quad (1.4)$$

将 NMOS 开关分为打开 (on) 和关闭 (off) 两种状态进行分别处理：

(1) NMOS off ($nT \leq t \leq (n + \frac{1}{2})T$)

NMOS 关闭，此时器件的电压 $v_{doff}(t)$ 和电流 $i_{doff}(t)$ 可以用电容 C_1 来表示：

$$i_{doff}(t) = C_1 \frac{dv_{doff}(t)}{dt} \quad (1.5)$$

将方程(1.5)带入 (1.3) 和(1.4)可得二阶微分方程：

$$L_1 C_1 \frac{d^2 i_{Loff}(t)}{dt^2} + i_{Loff}(t) = I_o \sin(\omega_c t + \phi_0) \quad (1.6)$$

解方程可得：

$$i_{Loff}(t) = A \cos(\omega_0 t) + B \sin(\omega_0 t) + \frac{I_o}{1 - \beta^2} \sin(\omega_c t + \phi_0) \quad (1.7)$$

其中， $\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$ ， $\beta = \frac{\omega_c}{\omega_0}$ ，A 和 B 为两个待定的恒定参数。

(2) NMOS on ($(n + \frac{1}{2})T \leq t \leq (n + 1)T$)

NMOS 打开，此时器件的电压 $v_{don}(t)$ 和电流 $i_{don}(t)$ 可以用 NMOS 导通电阻 R_{on} 来表示：

$$v_{don}(t) = i_{don}(t) R_{on} \quad (1.8)$$

将方程 (1.8) 带入 (1.3) 和(1.4)可的一阶微分方程：

$$V_{DD} - i_{Lon}(t) R_{on} + I_o R_{on} \sin(\omega_c t + \phi_0) = L_1 \frac{di_{Lon}(t)}{dt} \quad (1.9)$$

解方程可得：

$$i_{Lon}(t) = \frac{I_o \gamma}{\gamma^2 + \omega_c^2} [\gamma \sin(\omega_c t + \phi_0) - \omega_c \cos(\omega_c t + \phi_0)] + \frac{V_{DD}}{R_{on}} + C e^{-\gamma t} \quad (1.10)$$

其中， $\gamma = \frac{R_{on}}{L_1}$ ，C 为待定的恒定参数。

为了确定以上分析中的待定参数，需要借助周期性条件、边界条件等：

➤ 周期性条件:

$$\begin{cases} i_{Lon}(t)|_{t=(n+1)T} = i_{Loff}(t)|_{t=nT} \\ v_{don}(t)|_{t=(n+1)T} = v_{doff}(t)|_{t=nT} \end{cases} \quad (1.11)$$

➤ 边界条件

$$i_{Lon}(t)|_{t=(n+1/2)T} = i_{Loff}(t)|_{t=(n+1/2)T} \quad (1.12)$$

➤ Class E 条件:

$$\begin{cases} v_{doff}(t)|_{t=(n+1/2)T} = 0 \\ \frac{dv_{doff}(t)}{dt}|_{t=(n+1/2)T} = 0 \end{cases} \quad (1.13)$$

结合以上边界条件及所有方程，可到如下所示方程组:

$$\begin{cases} \frac{V_{DD}}{R_{on}} + Ce^{-\gamma T} + \frac{I_o \gamma}{(\gamma^2 + \omega_c^2)} (\gamma \sin \phi_0 - \omega_c \cos \phi_0) = A + \frac{I_o \sin \phi_0}{(1 - \beta^2)} \\ \frac{\gamma}{\omega_c} Ce^{-\gamma T} - \frac{I_o \gamma}{(\gamma^2 + \omega_c^2)} (\gamma \cos \phi_0 + \omega_c \sin \phi_0) = -\frac{B}{\beta} - \frac{I_o \cos \phi_0}{(1 - \beta^2)} \\ \frac{V_{DD}}{R_{on}} + Ce^{-\gamma T/2} - \frac{I_o \gamma}{(\gamma^2 + \omega_c^2)} (\gamma \sin \phi_0 - \omega_c \cos \phi_0) = A \cos \frac{\pi}{\beta} + B \sin \frac{\pi}{\beta} - \frac{I_o \sin \phi_0}{(1 - \beta^2)} \\ \frac{1}{\gamma} \left(A \omega_0 \sin \frac{\pi}{\beta} - B \omega_0 \cos \frac{\pi}{\beta} + \frac{I_o \omega_c}{(1 - \beta^2)} \cos \phi_0 \right) = -\frac{V_{DD}}{R_{on}} \\ Ce^{-\gamma T/2} + \frac{I_o \omega_c}{(\gamma^2 + \omega_c^2)} (\gamma \cos \phi_0 + \omega_c \sin \phi_0) = -\frac{V_{DD}}{R_{on}} \end{cases} \quad (1.14)$$

这里， V_{DD} 、 T 和 ω_c 由设计指标确定， β 和 γ 是 L_1 和 C_1 的函数， R_{on} 和 C_1 则由器件尺寸所决定。

功率放大器的直流耗散功率为:

$$P_{dc} = V_{DD} I_{dc} = P_{out} + P_d \quad (1.15)$$

其中,

$$I_{dc} = \frac{1}{T} \int_{nT}^{(n+1)T} i_L(t) dt = \frac{1}{T} \left(\int_{nT}^{(n+1/2)T} i_{Loff}(t) dt + \int_{(n+1/2)T}^{(n+1)T} i_{Lon}(t) dt \right) \quad (1.16)$$

$$P_d = \frac{1}{T} \int_{(n+1/2)T}^{(n+1)T} i_{don}^2(t) R_{on} dt \quad (1.17)$$

$$\frac{V_{DD}}{T} \left(\int_{nT}^{(n+1/2)T} i_{Loff}(t) dt + \int_{(n+1/2)T}^{(n+1)T} i_{Lon}(t) dt \right) = P_{out} + \frac{1}{T} \int_{(n+1/2)T}^{(n+1)T} i_{don}^2(t) R_{on} dt \quad (1.18)$$

在 (1.14) 和 (1.18) 中，六个方程中包含八个未知变量： A 、 B 、 C 、 ϕ_0 、 I_o 、 γ 、 β 和 R_{on} 。当工艺技术和 NMOS 的栅宽确定时， R_{on} 和 C_1 确定，则可以用以上六个方程解

得六个未知独立变量： A 、 B 、 C 、 ϕ_0 、 I_o 和 L_1 。

以上所述为设计 CMOS Class E 功率放大器的一套设计步骤，实验证明这些方程所描述的结果与实际仿真结果可以较好拟合。但是，需要注意的是，以上分析都基于三个基本假设，而这三个假设是不完全成立的。譬如，实际中 NMOS 关闭时其电容 C_1 并不是恒定的，而与漏极电压 $v_d(t)$ 相关。这些假设会给分析引入一定的误差，但仍然不失为设计 CMOS Class E 功率放大器很好的开始。

关于 NMOS 器件栅宽的选择：

As can be seen in (1.17): the power dissipated in the device is proportional to the switching-on resistance R_{on} , and the wider the device is, the smaller R_{on} . Therefore, it is not surprising that the efficiency is improved when a wider devices is employed. As the NMOS width increases, several practical issues arise. First, designing the driving stage becomes more and more difficult because of the increase of the gate capacitance. Second, the optimum drain inductance becomes very small, resulting in difficulties in practical implementation. Therefore, trade-offs have to be made in choosing the optimum NMOS width.

More about Class E Power Amplifier:

1. Simulation and verification tests on actual amplifiers seem to support the view that Class E does truly represent an alternative to conventional reduced conduction angle operation, giving higher efficiency without the circuit complexity of more advanced Class F designs. Class F can achieve very high efficiency, but show substantial reduced power output under optimum efficiency operation. Class E has its own disadvantage in terms of peak voltage levels, and the RF PUF has to be traded against this limitation. But the final judgment may be that Class E appears to be easier to realize in practice using solid state transistors than a short conduction angle Class C design.
2. The Class E mode may just represent a possibility for achieving high enough efficiencies from solid state devices that envelope restoration and outphasing may become mainstream techniques once again.
3. The main action of a Class E amplifier takes place within, and is indeed critically dependent on, the knee region of the I-V characteristic; the true-on is largely implemented by the turn-off is more conventionally implemented by using the transconductive pinchoff. This is a subtle point which partially explains the widespread belief that Class E cannot be made to work at GHz frequencies due to the slow and symmetrical transconductive switching characteristics of RF power transistors.
4. Class E: Theoretical efficiencies of around 90% can be achieved, albeit with an RF output power as much as 3dB lower than that obtainable from the same device in a conventional Class AB configuration. Class E amplifiers are highly nonlinear, but offer possibilities for envelope restoration techniques. On the downside, peak voltages can be as high as three times the DC supply if the power shortfall is to be kept within reasonable limits. There is also the issue of power gain. If a typical Class E amplifier is running at 3-5dB lower power gain, due to the overdrive requirement on the input, than a comparable linear amplifier, the upper

frequency limit will be lower for a given technology. Generally speaking, 12-13dB of linear gain would be required from a given device in order to stand a chance of useful Class E operation; however, the same can be said of conventional high efficiency modes with shorter conduction angles.

5. The really critical advantage of the Class E amplifier is efficiency, and with the possibility of reaching into the 90% range, the advantages of low heat generation offer some novel concepts in packaging, modulation, and power combining.

Reference

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2. Steve C. Cripps, “*RF Power Amplifiers for Wireless Communications*” 2nd Edition, Artech House, 2006